In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A method of performing a dot product operation with rounding and shifting in a microprocessor in response to a single rounding dot product instruction, the method comprising the steps of:

fetching a first pair of elements and a second pair of elements;

forming a first product of the first pair of elements and a second product of the second pair of elements;

~~combining the first product with the second product to form a combined product;~~

combining the first product with the second product to form a combined product and rounding the combined product to form an intermediate result via an arithmetic circuit having a first input receiving said first product, a second input receiving said second product and a carry input to a mid-position receiving said rounding value to form the intermediate result; and

right shifting the intermediate result a selected amount to form a final result.

Claims 2 and 3. (Canceled)

4. (Currently Amended) The method of Claim ~~3~~ 1, wherein the rounding value is 2^n and the selected shift amount is n+1.

5. (Original) The method of Claim 4, wherein n has a fixed value of fifteen.

Claims 6 to 8. (Canceled)

9. (Currently Amended) The method of Claim 1, wherein the ~~step~~ steps of forming the first product and forming the second product treats a one of the first pair of elements as a signed number value and treats another one of the first pair of elements as an unsigned number value.

10. (Original) The method of Claim 1, wherein the step of combining comprises subtracting the product of second pair of elements from the product of first pair of elements.

11. (Original) The method of Claim 1, wherein the step of combining comprises adding the product of second pair of elements to the product of first pair of elements.

12. (Canceled)

13. (Currently Amended) A digital system having a microprocessor operable to execute a rounding dot product instruction, wherein the microprocessor comprises:

storage circuitry for holding pairs of elements;

a multiply circuit connected to receive a first number of pairs of elements from the storage circuitry in a first execution phase of the microprocessor responsive to the dot product instruction, the multiply circuit comprising a plurality of multipliers equal to the first number of pairs of elements;

an arithmetic circuit having a plurality of inputs each connected to receive a corresponding one of the plurality of products from the plurality of multipliers~~, the arithmetic circuit having a provision~~ and a mid-position carry input for mid-position rounding responsive to the rounding dot product instruction; and

a shifter connected to receive an output of the arithmetic circuit, the shifter operable to shift a selected amount in response to the rounding dot product instructions.

Claims 14 and 15. (Canceled)

16. (Currently Amended) The method of Claim ~~3~~ 1, wherein:
the step of shifting further includes sign ~~extends~~ extending the intermediate result.

17. (New) The digital system of Claim 13, wherein:
the shifter right shifts the output of the arithmetic circuit by the selected amount and sign extends the output of the arithmetic circuit.

18. (New) A method of performing a dot product operation with rounding and shifting in a microprocessor in response to a single rounding dot product instruction, the method comprising the steps of:
fetching a first pair of elements and a second pair of elements;
forming a first product of the first pair of elements treating a one of the first pair of elements as a signed number value and treating another one of the first pair of elements as an unsigned number value;
forming a second product of the second pair of elements treating a one of the first pair of elements as a signed number value and treating another one of the first pair of elements as an unsigned number value;
combining the first product with the second product to form a combined product;

rounding the combined product to form an intermediate result; and

shifting the intermediate result a selected amount to form a final result.

19. (New) The method of Claim 18, wherein the step of rounding adds a rounding value to the combined product via an arithmetic circuit having a first input receiving said first product, a second input receiving said second product and a carry input to a mid-position receiving said rounding value to form the intermediate result, and wherein the step of shifting shifts the intermediate result right by a selected shift amount.

20. (New) The method of Claim 19, wherein the rounding value is 2^n and the selected shift amount is n+1.

21. (New) The method of Claim 20, wherein n has a fixed value of fifteen.

22. (New) The method of Claim 19, wherein:

the step of shifting further includes sign extending the intermediate result.

23. (New) The method of Claim 18, wherein the step of combining comprises subtracting the product of second pair of elements from the product of first pair of elements.

24. (New) The method of Claim 18, wherein the step of combining comprises adding the product of second pair of elements to the product of first pair of elements.